ABSTRACT OF THE DISCLOSURE

A semiconductor device has a lower metal layer, a lower dielectric layer on top of the lower metal layer, an upper metal layer on top of the lower dielectric layer, an upper dielectric layer on top of the upper metal layer, and a contact region formed as a cavity that extends through the upper dielectric layer, the upper metal layer and the lower dielectric layer for access to a solder pad portion of the lower metal layer. A dielectric lining layer lines a peripheral cavity-confining surface of the cavity, and is transverse to a plane of the lower metal layer. The dielectric lining layer isolates the upper metal layer from the lower metal layer while permitting access to the solder pad portion of the lower metal layer. An electrical contact fills the cavity, and enables external electrical connection with the lower metal layer.